## AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

## Listing of Claims:

1. (Currently amended) A semiconductor device comprising:

a first semiconductor region of a first conductivity type, defined by an upper end surface, a lower end surface opposing to the upper end surface, and first and second side boundary surfaces connecting the upper and lower end surfaces when viewed in section;

a second semiconductor region of the first conductivity type disposed under the first semiconductor region and being in ~~metallurgical~~ contact with said first semiconductor region ~~at~~ so as to have the lower end surface as a common tangent plane between the first and second semiconductor regions;

a third semiconductor region of a second conductivity type disposed on the first semiconductor region and being in ~~metallurgical~~ contact with said first semiconductor region ~~at~~ so as to have the upper end surface as a common tangent plane between the first and third semiconductor regions; and

a fourth semiconductor region having first and second inner surfaces in ~~metallurgical~~ contact with the first and second side boundary surfaces respectively when viewed in section and an impurity concentration lower than said first semiconductor region, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions.

2. (Original) The semiconductor device of Claim 1, wherein said fourth semiconductor region has the first conductivity type.

3. (Previously presented) The semiconductor device of Claim 1, wherein outer surface of said fourth semiconductor region serves as a chip outer-surface of the semiconductor device and the chip outer-surface is substantially orthogonal with the lower end surface of said first semiconductor region.

4. (Original) The semiconductor device of Claim 1, wherein said fourth semiconductor region is made of a wafer cut from bulk crystal.

5. (Previously presented) The semiconductor device of Claim 1, further comprising a first main electrode layer formed on a bottom surface of said second semiconductor region.

6. (Previously presented) The semiconductor device of Claim 5, wherein said first main electrode layer is contacted with said second semiconductor region, through a first concavity formed at the bottom surface of said semiconductor region.

7. (Previously presented) The semiconductor device of Claim 1, further comprising a first main electrode layer, a part of the first main electrode layer being buried in a via hole penetrating through said second semiconductor region, configured such that the buried part of the first main electrode layer contacts with said first semiconductor region.

8. (Previously presented) The semiconductor device of Claim 1, further comprising a second main electrode layer formed on a top surface of said third semiconductor region.

9. (Previously presented) The semiconductor device of Claim 8, wherein said second main electrode layer is contacted with said third semiconductor region, through a second concavity formed at the top surface of said third semiconductor region.

10. (Cancelled).

11. (Cancelled).

12. (Withdrawn).

13. (Withdrawn).